Attorney's Docket No.: Intel P17483 / 10559-881001

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: COMPOSITE OPTICAL LITHOGRAPHY METHOD FOR PATTERNING LINES OF SUBSTANTIALLY EQUAL WIDTH

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CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV 399290763 US

October 7, 2003

Date of Deposit

COMPOSITE OPTICAL LITHOGRAPHY METHOD FOR PATTERNING LINES OF SUBSTANTIALLY EQUAL WIDTH

BACKGROUND

[0001] An integrated circuit (IC) manufacturing process may deposit various material layers on a wafer and form a photosensitive resist (photoresist) on the deposited layers. The process may use lithography to transmit light through or reflect light from a patterned reticle (mask) to the photoresist. Light from the reticle transfers a patterned image onto the photoresist. The process may remove portions of the photoresist which are exposed to light. A process may etch portions of the wafer which are not protected by the remaining photoresist to form integrated circuit features.

[0002] The semiconductor industry may continually strive to reduce the size of transistor features to increase transistor density and to improve transistor performance. This desire has driven a reduction in the wavelength of light used in photolithographic techniques to define smaller IC features in a photoresist. Complex lithographic exposure tools may cost more to make and operate.

[0003] A conventional patterning technique may use expensive, diffraction-limited, high numerical aperture (NA), highly aberration corrected lens/tools equipped with complex

illumination. A conventional patterning technique may also use complicated and expensive masks, which employ various phase shifters and complex optical proximity (OPC) corrections.

BRIEF DESCRIPTION OF DRAWINGS

[0004] Fig. 1A illustrates an interference lithography apparatus.

[0005] Fig. 1B illustrates an example of a diffraction grating with slits which allow light to pass through and radiate a photoresist on a substrate.

[0006] Fig. 2 illustrates a latent or real image of a pattern of spaces and lines produced by the interference lithography apparatus of Fig. 1A or by projecting an image of a grating in Fig. 1B through projection optics onto the substrate.

[0007] Fig. 3A illustrates an example of a desired layout of integrated circuit features formed by an interference lithography process and a second lithography process.

[0008] Fig. 3B illustrates an example of the second lithography process layout which may expose desired areas of the photoresist to radiation, which breaks continuity of the patterned lines of Fig. 2 to produce the desired layout of Fig. 3A.

[0009] Figs. 4A-4H illustrate an example of a second lithography process to expose areas on a photoresist and subsequent processes of developing, etching and stripping.

[0010] Fig. 5 illustrates a composite optical lithography exposure system with a movable wafer stage.

[0011] Fig. 6 shows an optical lithographic implementation of the second patterning system.

[0012] Fig. 7 is a flow chart of the composite optical lithography patterning technique.

[0013] Fig. 8 shows a process for generating a layout of a mask for the second lithography process.

[0014] Fig. 9 shows an example of a design layout.

[0015] Fig. 10 shows an example of a remainder layout.

[0016] Fig. 11 shows a remainder layout after an expansion in a direction D.

DETAILED DESCRIPTION

[0017] The present application relates to a composite optical lithography patterning technique, which may form smaller integrated circuit features compared to conventional lithography techniques. The composite patterning technique may provide a high density of integrated circuit features for a given area on a substrate.

[0018] The composite patterning technique may include two lithography processes. A first lithography process uses a radiation source and an interference lithography apparatus to form a pattern of alternating lines and spaces on a photosensitive media. A second lithography process may use one or more non-interference lithography techniques, such as projection optical lithography, imprint lithography and electron-beam (e-beam) lithography, to break continuity of the patterned lines and form desired integrated circuit features.

[0019] In another embodiment, the first process may include a non-interference lithography technique, and the second process may include an interference lithography technique.

[0020] **First Lithography Process**

[0021] Fig. 1A illustrates an interference (interferometric) lithography apparatus 100. The interference lithography apparatus 100 may include a beam splitter 104 and two mirrors 106A, 106B. The beam splitter 104 may receive radiation, such as conditioned (expanded and collimated) laser beam 102, from a radiation source with a pre-determined exposure wavelength (λ). The beam splitter 104 may direct the radiation 102 to the mirrors 106A, 106B. The mirrors 106A, 106B may form a pattern 200 (Fig. 2) on a substrate 108 with a photosensitive media, such as a photoresist layer 107. Many interferometric lithography tool designs with various complexity and

sophistication are available. Either a positive or a negative photoresist may be used with the processes described herein. θ may be an angle between a surface normal of the photoresist 107 and a beam of radiation incident on the photoresist 107.

[0022] Fig. 2 illustrates a latent or real image of pattern 200 of alternating spaces 204 (exposed to light) and lines 202 (not exposed to light) produced by the interference lithography apparatus 100 of Fig. 1A. "Latent" refers to a pattern on the photoresist 107 which experienced a chemical reaction due to radiation but has not yet been developed in a solution to remove the exposed areas of positive tone photoresist 107 (Fig. 4C described below). The lines 202 may have a substantially equal width. The spaces 204 may or may not have a width equal to the width of the lines 202.

[0023] "Pitch" is a sum of a line width and a space width in Fig. 2. As known to those of ordinary skill in optics, a "minimal pitch," which can be resolved by a projection optical exposure apparatus with a pre-determined wavelength λ and numerical aperture NA, may be expressed as:

[0024] $\text{pitch}/2 = (k_1(\lambda/ni))/NA$

"NA" is the numerical aperture of a projection lens in the lithography tool. "ni" is the refractive index of a media between the substrate 108 and the last element of the optical projection system, e.g., mirrors 106A, 106B. Optical projection

systems currently in use for microlithography use air, which has ni = 1. ni > 1.4 for liquid immersion microlithographic systems. For ni = 1, the pitch may be expressed as:

[0025] $pitch/2 = k_1\lambda/NA$

[0026] $pitch = 2k_1\lambda/NA$

[0027] NA may be expressed as:

[0028] $NA = n_0 \sin\theta$

[0029] NA may be equal to 1. k_1 may be known as a Rayleigh's constant.

[0030] If $k_1 = 0.25$, and n_0 is about equal to one, pitch may expressed as:

[0031] $pitch = 2(.25)\lambda/n_0\sin\theta \cong \lambda/2\sin\theta$

[0032] Other values of k_1 may be greater than 0.25.

[0033] The interference lithography apparatus 100 of Fig. 1A may achieve a "minimal pitch" (a minimal line width plus space width) expressed as:

[0034] $minimal\ pitch \cong \lambda/2$

[0035] The lines 202 and spaces 204 may have a pitch P_1 approaching $\lambda_1/2$, where λ_1 is the radiation wavelength used in the interference lithography process. The wavelength λ_1 may equal to 193 nm, 157 nm or an extreme ultraviolet (EUV) wavelength, such as 11-15 nm or any other wavelength suitable for patterning microlithography patterns with the help of

interferometic lithography. Larger pitches may be obtained by changing the angle θ of interfering beams in Fig. 1A.

[0036] Minimal feature size of an exposed space 204 or non-exposed line 202 may be equal to, less than or larger than exposure wavelength divided by four (λ/4).

[0037] The first (interference lithography) process may define a width of all minimal critical features of a final pattern at a maximum density achievable by means of optical patterning with maximum process latitude.

[0038] Instead of the beam splitter 104, any light-splitting or interference element may be used, such as a prism or diffraction grating, to produce a pattern 200 of alternating lines 202 and spaces 204 on the photoresist 107.

[0039] Fig. 1B illustrates an example of a diffraction grating 120 with slits 122 which allow light to pass through and radiate a photoresist 107 on a substrate 108. The diffraction grating 120 in conjunction with projection optics may produce the same pattern 200 (Fig. 2) as the beam splitter 104 and mirrors 106A, 106B of Fig. 1A.

[0040] The area of the pattern 200 formed by interference lithography may be equal to a die, multiple dies or a whole wafer, e.g., a 300-mm wafer or even larger future generation wafer sizes. Interference lithography may have excellent

dimensional control of a pattern 200 due to a large depth of focus.

[0041] Interference lithography may have a lower resolution limit and better dimensional control than projection (lens-based) lithography. Interference lithography may have a higher process margin than projection lens-based lithography because depth of focus for interference lithography may be hundreds or thousands of microns, in contrast to a fraction of a micron (e.g., 0.3 micron) depth of focus for some conventional optical lithography techniques. Depth of focus may be important in lithography because focus control of exposure systems at sub-micron level is not sufficiently stable. In addition, the photoresist may not be completely flat because (a) the photoresist is formed over one or more metal layers and dielectric layers or (b) semiconductor wafer itself might not be sufficiently flat.

[0042] An embodiment of interference lithography may not need a complicated illuminator, expensive lenses, projection and illumination optics or a complex mask, in contrast to other lithography techniques.

[0043] **Second Lithography Process**

[0044] A second lithography process may include one or more non-interference lithography techniques, such as a conventional lithography technique, such as projection optical lithography,

imprint lithography and electron-beam (e-beam) lithography. Alternatively, the second lithography process may use extreme ultraviolet (EUV) lithography.

[0045] Fig. 3A illustrates an example of a desired layout 300 of integrated circuit features formed by the interference lithography process described above and a selected second lithography process.

[0046] Fig. 3B illustrates an example of the second lithography process layout 320 that may expose desired areas 302 of the photoresist 107 to radiation, which breaks continuity of the patterned lines 202 of Fig. 2 to produce the desired layout 300 shown on Fig. 3A. The layout 320 of Fig. 3B may be an oblique mask with transmissive openings 332 for positive resist imaging. Alternatively, the layout 320 of Fig. 3B may be a non-reflective mask with reflective openings 332. A method for making a print mask is described below with reference to Figs. 8-12.

[0047] The second lithography process may remove or erase undesired portions 302 of the lines 202, which were not exposed to light during the first process, by exposing the undesired portions of the lines 202 to radiation. Thus, the spaces 204 and areas 302 in Figs. 3A-3B are exposed to light during the first and second processes, respectively.

[0048] λ_1 may represent a radiation wavelength used in the first (interference) lithography process, and λ_2 represents a radiation wavelength used in the second (conventional) lithography process. For example, the wavelengths λ_1 and λ_2 may each be 193 nm, 157 nm or an extreme ultraviolet (EUV) wavelength, such as 11-15 nm.

[0049] The patterning layout of the second lithography process on an exposure mask (or maskless patterning tool database) may be a Boolean difference between (a) a desired final pattern shown in Fig. 3A, which is sized up for desired dimensional and overlay controls for all minimal line-width features, and (b) the diffraction grating pattern 200 (Fig. 2) formed by the first lithography process. Approximate layout of the second process' mask (or its corresponding database for maskless patterning) is shown as areas 302 in Fig. 3B.

[0050] As shown in Fig. 3A, the layout 300 formed by the first and second processes may be limited to the minimal pitch (P) of the continuous alternating lines and spaces pattern 200 in Fig. 2 and integer multiples of the minimal pitch (e.g., 1P, 2P, 3P).

[0051] Figs. 4A-4H illustrate an example of a second lithography process to expose areas 302 (Fig. 3) on the photoresist 107 and subsequent processes of developing, etching and stripping. A photoresist 107 may be formed (e.g., coated)

on a substrate 108 in Fig. 4A. A latent or real pattern 200 of alternating continuous lines and spaces (unexposed and exposed regions)(Fig. 2) may be formed on the photoresist 107 by the interference lithography apparatus 100 of Fig. 1A. A second lithography tool (second lithography process) may transmit light 403 through a patterned mask or reticle 404 to expose desired areas 302 of the photoresist 107 in Fig. 4B. The light 403 may start a reaction in the exposed areas 302. The light 403 may be Ultraviolet or extreme ultraviolet (EUV) radiation, for example, with a wavelength of about 11-15 nanometers (nm).

[0052] The photoresist 107 and substrate 108 may be removed from the lithography tool and baked in a temperature-controlled environment. Radiation exposure and baking may change the solubility of the exposed areas 302 and spaces 204 (Fig. 2) compared to unexposed areas of the photoresist 107. The photoresist 107 may be "developed," i.e., put in a developer and subjected to an aqueous (H2O) based solution, to remove exposed areas 302 and spaces 204 of the photoresist 107 in Fig. 4C to form a desired pattern in the resist. If a "positive" photoresist is used, exposed areas 302 and 204 may be removed by the solution. Portions 410 of the substrate 108 which are not protected by the remaining photoresist 107 may be etched in Fig. 4D to form desired circuit features. The remaining photoresist 107 may be stripped in Fig. 4E.

[0053] If a "negative" photoresist is used, areas which are not exposed to radiation may be removed by the developing solution, as shown in Fig. 4F. Then portions 420 of the substrate 108 which are not protected by the remaining photoresist 422 may be etched in Fig. 4G to form desired circuit features. The remaining photoresist 422 may be stripped in Fig. 4H.

[0054] To break continuity of lines 202 to form desired layout shown in Fig. 3A, a conventional lithography exposure tool may be used. Integrated circuit layouts customary used in patterning lines produce a pattern with a length-to-width ratio of equal or greater than 1.5:1 (e.g., for a gate layer of a transistor structure). Thus, a conventional exposure tool may be used to form the areas 302 of Fig. 3 because pitch for "along length" areas 302 may be about 1.5 or more times larger than for minimal features, such as the exposed spaces 204. The areas 302 produced by a conventional exposure tool produce a "cut," which may be reduced further through the use of known RELACS™ or SAFIRE™ size reduction techniques. A simple binary mask with minimal proximity correction may be used in the second lithography process.

[0055] For example, 193-nm interference tool may produce a 100-nm pitch grating pattern, while 193-nm or 248nm or 365nm

optical projection tools may be used for a second lithography process to pattern line-to-line openings.

[0056] The second lithography process may use another mask-based technique such as imprint or a maskless patterning technique.

[0057] Combining an interference lithography technique and a non-interference technique may provide high IC pattern density scaling (patterning at k1 = 0.25 for any available wavelength).

[0058] Interference lithography, which patterns minimal pitch features, may extend 193-nm immersion lithography to 66-nm pitch and may extend an EUV interference tool capability down to 6.7-nm pitch.

[0059] Interference lithography may have an all-reflective design, e.g., Lloyds' mirror interferometric lithographic system, which may enable system design with available wavelengths between 157 nm and 13.4 nm, such as a neon discharge source (about 74-nm wavelength) and a helium discharge source (58.4-nm wavelength) with corresponding minimal pitches of 37 nm and 30 nm, respectively.

[0060] Fig. 7 is a flow chart of the composite optical lithography patterning technique. Interference lithography exposure on a photoresist at 700 may be followed by a second lithography exposure applied to the same photoresist at 702. The photoresist may be baked, and soluble portions of the

photoresist may be developed at 704 if the photoresist is sensitive to both interference lithography and the second lithography exposure wavelength(s).

[0061] Alternatively, the interference lithography exposure may be followed by developing the photoresist. After development, the second lithography process may be preceded by applying a second patterning media layer, which may be a different photosensitive media than the first photoresist. The selected second lithography process may determine which patterning media is selected, such as an electron beam sensitive resist or a photosensitive imprint media for imprint patterning. Depending on the selected second lithography process (e.g., optical, imprint, e-beam, etc.), the continuity of the patterned lines 202 (Fig. 2) in the first photoresist 107 may be destroyed by etching portions of the lines 202 defined by the first photoresist 107 through an opening in the patterned media produced by second layer processing.

[0062] **Alignment**

[0063] An existing alignment sensor (not shown) on the interference lithography apparatus 100 may align the pattern 200 (Fig. 2) produced by the first lithography process to a previous layer pattern formed by other processes. An existing alignment sensor may be above a wafer and be adapted to sense a mark on the wafer.

[0064] Alignment of the second lithography process to the first lithography process may be achieved by either indirect alignment (second lithography process aligns to previous layer pattern by means of existing alignment sensors) or direct alignment (second lithography process aligns to first lithography process pattern 200 directly) by means of a latent image alignment sensor.

[0065] Fig. 5 illustrates a composite optical lithography system 500 with a movable wafer stage 545. The composite optical lithography system 500 may include an environmental enclosure 505, The enclosure 505 encloses an interference lithography system 510 and a second (non-interference) patterning system 515. The interference lithography system 510 may include a collimated coherent radiation source 520 and interference optics 525 to provide interferometric patterning of desired area on a photoresist.

[0066] The second patterning system 515 may use one of several techniques to pattern a photoresist. For example, the second patterning system 515 may be an e-beam projection system, an imprint printing system, or an optical lithography system. Alternatively, the second patterning system 515 may be a maskless module, such as an electron beam direct write module, an ion beam direct write module, or an optical direct write module.

[0067] The two systems 510, 515 may share a common mask handling subsystem 530, a common wafer handling subsystem 535, a common control subsystem 540, and a common stage 545. The mask handling subsystem 530 may position a mask in the system 500. The wafer handling subsystem 535 may position a wafer 561 in the system 500. The control subsystem 540 may regulate one or more properties or devices of system 500 over time. For example, the control subsystem 540 may regulate the position, alignment or operation of a device in system 500. The control subsystem 540 may also regulate a radiation dose, focus, temperature or other environmental qualities within environmental enclosure 505.

[0068] The control subsystem 540 can also translate the stage 545 between a first exposure stage position 555 and a second exposure stage position 550. The stage 545 includes a wafer chuck 560 for gripping a wafer 561. At the first position 555, the stage 545 and the chuck 560 may present a gripped wafer 561 to the interference lithography system 510 for interferometric patterning. At the second position 550, the stage 545 and the chuck 560 may present the gripped wafer 561 to the second patterning system 515 for patterning.

[0069] To ensure the proper positioning of a wafer 561 by the chuck 560 and the stage 545, the control subsystem 540 may include an alignment sensor 565. The alignment sensor 565 may transduce and control the position of the wafer 561 (e.g., using

wafer alignment marks) to align a pattern formed by the second patterning system 515 with a pattern formed by the interference lithography system 510. Such positioning may be used when introducing irregularity into a repeating array of interferometric features, as discussed above.

[0070] Fig. 6 shows an optical lithographic implementation of the second patterning system 515. In particular, the second patterning system 515 may be a step-and-repeat projection system. Such a patterning system 515 may include an illuminator 605, a mask stage 610, a mask 630 and projection optics 615. The illuminator 605 may include a radiation source 620 and an aperture/condenser 625. The radiation source 620 may be the same as radiation source 520 in Fig. 5. Alternatively, the radiation source 620 may be a separate device. The radiation source 620 may emit radiation at the same or at a different wavelength as the radiation source 520.

[0071] The aperture/condenser 625 may include one or more devices for collecting, collimating, filtering, and focusing the emitted radiation from the radiation source 520 to increase the uniformity of illumination upon mask stage 610. The mask stage 610 may support a mask 630 in the illumination path. The projection optics 615 may reduce image size. The projection optics 615 may include a filtering projection lens. As the stage 545 translates a gripped wafer 561 for exposure by the

illuminator 605 through mask stage 610 and projection optics 615, the alignment sensor 565 may ensure that the exposures are aligned with a repeating array 200 of interferometric features to introduce irregularity into the repeating array 200.

[0072] Fig. 8 shows a process 800 for generating a layout of a mask for the second lithography process described above. The process 800 may be performed by one or more actors (such as a device manufacturer, a mask manufacturer, or a foundry) acting alone or in concert. The process 800 may also be performed in whole or in part by a data processing device executing a set of machine-readable instructions.

[0073] The actor performing the process 800 receives a design layout at 805. The design layout is an intended physical design of a layout piece or substrate after processing. Figs. 3A and 9 show examples of such design layouts 300, 900. The design layout 300, 900 may be received in a machine-readable form. The physical design of the layout 300, 900 may include a collection of trenches and lands between the trenches. The trenches and lands may be linear and parallel. The trenches and lands need not repeat regularly across the entire layout piece. For example, the continuity of one or both of trenches and lands may be cut at arbitrary positions in the layout 300, 900.

[0074] Returning to Fig. 8, the actor performing the process 800 may also receive a pattern array layout 200 of alternating,

parallel lines 202 and spaces 204 (Fig. 2) at 810. The pattern array layout 200 may be formed on a photoresist 107 by interferometric lithography techniques, i.e., interference of radiation. The pattern array layout 200 may be received in a machine-readable form.

[0075] Returning to Fig. 8, the actor may subtract the design layout 900 (Fig. 9) from the pattern array layout 200 (Fig. 2) at 815. The subtraction of the design layout 900 from the pattern array layout 200 may include aligning trenches 332 in the design layout 900 with either lines or spaces in the pattern array layout 200 and determining positions where irregularity in the design layout 900 prevents complete overlap with the pattern array layout 200.

[0076] Figs. 3B and 10 show examples of remainder layouts 330, 1000 that indicate positions where the design layouts 300, 900 do not completely overlap with the pattern array layout 200 (Fig. 2). The remainders layouts 330, 1000 may be in machine-readable form. The subtraction may be Boolean because positions in the remainder layouts 330, 1000 may have only one of two possible states. In particular, the remainder layout 1000 includes expanses of first positions 1005 with a "not overlapped" state and a contiguous expanse of second positions 1010 with an "overlapped" state.

[0077] Returning to Fig. 8, the actor may resize expanses of positions in the remainder layout 1000 at 820. The resizing of the remainder layout 1000 may result in a changed machine-readable remainder layout 1100 in Fig. 11. Fig. 11 shows a remainder layout 1100 after such an expansion in a direction D. When the pattern array is an array 200 of parallel lines 202 and spaces 204, the size of expanses 1105 with a present state may be increased in the direction perpendicular to the lines 202 and spaces 204. Some expanses 1105 may merge.

[0078] Returning to Fig. 8, the actor may generate a print mask using the remainder layout 1000 in Fig. 10 at 825. The print mask may be generated using the resized remainder layout 1100 of Fig. 11 to create arbitrarily shaped features for introducing irregularity into a repeating array, such as the pattern array 200 (Fig. 2). The generation of the print mask may include generating a machine-readable description of the print mask. The generation of the print mask may also include tangibly embodying the print mask in a mask substrate.

[0079] Alternatively, if the second lithography process uses EUV wavelengths, elements of an EUV lithography system, including the mask to be used, may be reflective. The clear (transmissive) areas on a non-EUV mask will be reflective areas on a EUV mask, and opaque (chrome) areas on a non-EUV mask will be absorptive areas on an EUV mask.

[0080] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the application. Accordingly, other embodiments are within the scope of the following claims.